REMARKS

Applicant adds new claims 46-49; therefore, claims 1-17 and 42-49 are pending in this application.

New dependent claims 46-49 have been added more fully to cover additional features of Applicant's invention as described in the specification at, for example, pages 12-17, and illustrated, for example in Figs. 1C, 2 and 4.

The Examiner indicates that claims 4 and 8-14 would be allowable if rewritten in independent form including the limitations of the base claim and any intervening claims. However, the Examiner cites a new reference, U.S. Patent No. 6,287,890 to Ho, and rejects claims 1-3, 5-7, 15-17 and 42-45 under 35 U.S.C. § 103(a) as being anticipated by Ho[1].

Applicant respectfully traverses the Examiner's prior art rejection as follows.

As explained in Applicant's Amendment filed December 1, 2003, Applicant's invention provides semiconductor package boards having a unique combinations of features, including, *inter alia*: a multilayer wiring film having a first surface; the first surface having a first region in contact with a metal base plate; the first surface having a second region exposed by an opening

[1] Applicant notes that in the Office Action, paragraph 8, the Examiner states the "Ho fails to teach...claim 1". Clearly, in view of the Examiner's rejection of claim 1 (see Office Action, paragraph 5), and the portions of Ho cited by the Examiner at the end of paragraph 8, the Examiner intended to state that "Ho teaches ... claim 1". Applicant responds accordingly.

in the metal base plate; and a plurality of first metal pads formed in the second region (see Applicant's independent claims 1 and 45).

Contrary to the Examiner's analysis, Ho does not disclose, teach or suggest such features. Ho discloses a semiconductor device package having an interconnect substrate 12, a metal substrate 14 mounted on the interconnect substrate 12 and having an opening 28, and a wire bond chip or flip chip 16 mounted in the opening 28 (*see Id.*, col. 6, line 30 through col. 7, line 34; and Fig. 1).

In particular, Ho discloses a semiconductor device where:

> The interconnect substrate 12 that has two surfaces. The surface of the interconnect substrate into which the contact balls 10 are mounted is the first surface of the interconnect substrate. The surface of the interconnect that is in contact with the metal substrate 14 is the second surface of the interconnect substrate.
>
> The metal substrate 14 has two surfaces, the first surface 24 of the metal substrate 14 is the surface on which the interconnect substrate 12 is created. The second surface 26 of the metal substrate is the surface into which openings are etched for the insertion of wire bond chips.
>
> The metal layer within the interconnect substrate 12 that is closest to the first surface 24 of the metal substrate 14 is referred to as the bottom layer, the metal layer within the interconnect substrate 12 that is furthest removed from the first surface 24 of the metal substrate 14 is referred to as the top layer.
>
> The two interconnect layers within the interconnect substrate 12 are highlighted as 18 (which can be a ground or power layer) and 20 (which can be a signal layer). Metal substrate 14, typically copper, is between about 30 to 40 mils thick. The metal used for substrate 14 is not limited to copper but can be other metals such as aluminum or stainless steel.
>
> ...

> The wire bond chip or flip chip 16 is mounted in an opening 28 that has been created in the metal substrate 14. The opening 28 into which the wire bond chip or flip chip 16 is mounted is a cavity that is created by masking and etching of the second side 26 of the metal substrate 14.
>
> An epoxy thin film (not shown) is first deposited over the metal substrate 14 on the first side 24 of the metal substrate 14. This deposition of the epoxy can be done by either lamination of a dry film or by depositing a liquid film of epoxy (a coating and curing process).
>
> (*Id.*, col. 6, line 33 through col. 7, line 26).

According to Ho, interconnect metal layer 20 is formed on top of the epoxy layer, and consists of plate base 50 and interconnect pattern 54 coated with dielectric 58 (*See Id.*, col. 7, lines 35-57).[2] Ho describes a conventional methods of mounting a wire bond chip or a flip chip 16 in the opening 28 where:

> After the cavity 28 has been created in the second surface 26 of the metal substrate 14 (thereby exposing the layer of epoxy that has been deposited over the first surface 24 of the metal substrate), openings are created in the exposed layer of epoxy through which electrical contact is established with points of contact in the bottom layer 20 of the interface substrate 12. One large opening or a matrix of small openings are created in the exposed layer of epoxy on top of a metal die pad onto which the die is to be placed for the die bonding and for heat removal purposes. These openings are created using laser technology. For flip chip connection, a matrix of small openings is created in the epoxy layer to expose the flip chip bond pads underneath the epoxy layer. (Id., col. 8, line 61 through col. 9, line 6)

[2] Applicant notes that Ho does not describe layer labeled "51", shown in Figs. 2a-2f, anywhere in the patent.

In the case of a wire bond chip, as illustrated in Ho's Fig. 1, the surface of chip 16 having electrical contacts is facing "away" from the interconnect substrate 12. Wire bond chip 16 is "die bonded" to the bottom layer 20 such that "each chip pad is wire bonded [see Fig. 1, wire bonding 15] to the corresponding substrate pad". In the case of a flip chip, not illustrated, the surface of chip 16 having electrical contacts is facing "downward" toward the interconnect substrate 12. Flip chip 16 is "reflow bonded" to the bottom layer 20 such that "an underfill epoxy material is used to flow under the die and to seal the flip chip solder balls to enhance the reliability of the solder ball connection". (See Id., col. 9, lines 12-64.)

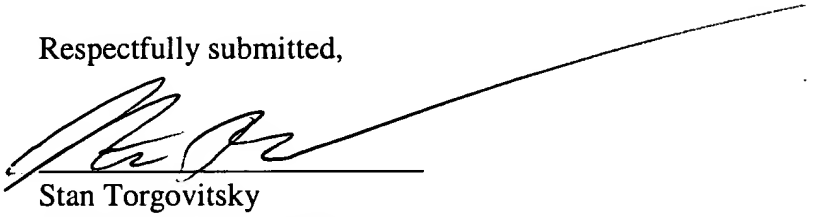
Nowhere does Ho disclose, teach or suggest that the "second surface" of its interconnect substrate 12 has metal pads formed in the region of the opening 28. That is, nowhere does Ho disclose, or suggest that either its "substrate pads" (for mounting a wire bond chip), or its "bond pads underneath the epoxy layer" (for mounting a flip chip), are metal pads formed in a region of the "second surface" of substrate 12 exposed by an opening 28 in the metal plate 14. Ho's Fig. 1, which shows the overall structure of the semiconductor device package, does not show any detail of the connection between chip 16 and bottom layer 20. However, Ho describes in great detail the formation of bottom layer 20 interconnect pattern 54 (see Figs. 2a-2f), which does not have any metal pads formed thereon.

Accordingly, Applicant's independent claims 1 and 45, as well as the dependent claims 2, 3, 5-7, 15-17 and 42-44 (which incorporate all the novel and unobvious features of their base claim), are not anticipated by (i.e., are not readable on) Ho at least for this reason.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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